A Hough Transform-Based Line Detection Accelerator

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I. INTRODUCTION

The Hough transform for line detection is widely used in many machine vision applications due to its robustness against data loss and distortion [1]. However, it is not appropriate for real-time embedded vision systems, because it has inefficient computation structure and demands a large number of memory accesses. Thus, there are some researches and developments for the implementation of hardware accelerators for line detection but they are only about line detection using FPGA devices which have constraints in cost and performance. On the other hand, there are few researches and developments for ASIC implementation of line detection accelerator. So, we developed a Hough transform-based line detection accelerator ASIC for low-power and small-area implementation.

II. DESCRIPTION

A. Description System Architecture

We improved the conventional voting scheme of the Hough transform, and then we applied this scheme to our Hough transform hardware architecture so that it can provide real-time performance with less hardware resource [2]. Fig. 1 shows the proposed voting scheme of the Hough transform. This scheme reduces computation overhead of the voting procedure by using correlation between adjacent pixels and by increasing reusability of vote values. The proposed hardware architecture maximizes its throughput by computing and storing vote values for many adjacent pixels in parallel.

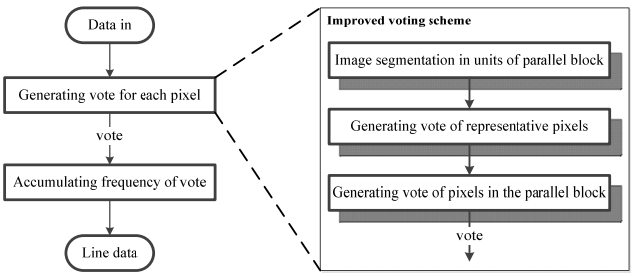

Fig. 1. Proposed voting scheme of the Hough transform.

B. Design and Implemention

The proposed Hough transform circuit was designed with Verilog HDL and verified by FPGA implementation, and then we compared the proposed method with the related work in the aspect of cost and performance [2][3].

III. CHIP IMPLEMENTAION AND RESULTS

After FPGA verification of the proposed Hough transform module, it was implemented in an ASIC through IDEC MPW with M/H 0.18 um technology. Table 1 shows the detailed specifications of the Hough transform ASIC, and Fig. 2 shows its layout and package.

Specifications	
Gate count	560,000
Frequncy	27 MHz
SRAM	46 SRAMSs of 1120 × 8
die size	4.5 mm × 4 mm
Package	LQFP 208

Table 1. Chip specifications.

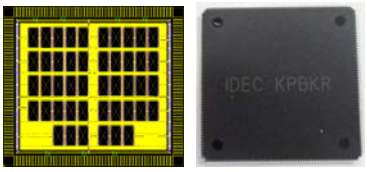

Fig. 2. Layout and package of the Hough transform ASIC.

REFERENCE

[1] C. T. Ho and L. H. Chen, "A high speed algorithm for line detection," *Pattern Recognition Lett.*, vol. 17, no. 5, pp. 467-473, May 1996.

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[3] Z. H. Chen, A. W. Y. Su, and M. T. Sun, "Resource-efficient FPGA architecture and implementation of hough transform," *IEEE Trans. VLSI Syst.*, vol. 20, no. 8, pp. 1419-1428, Aug. 2012.

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